FIG.1

High-level
hardware
description



Synthesis
tool

7



Target
hardware
model

Simulation
engine

8



Simulation
results

FIG.2

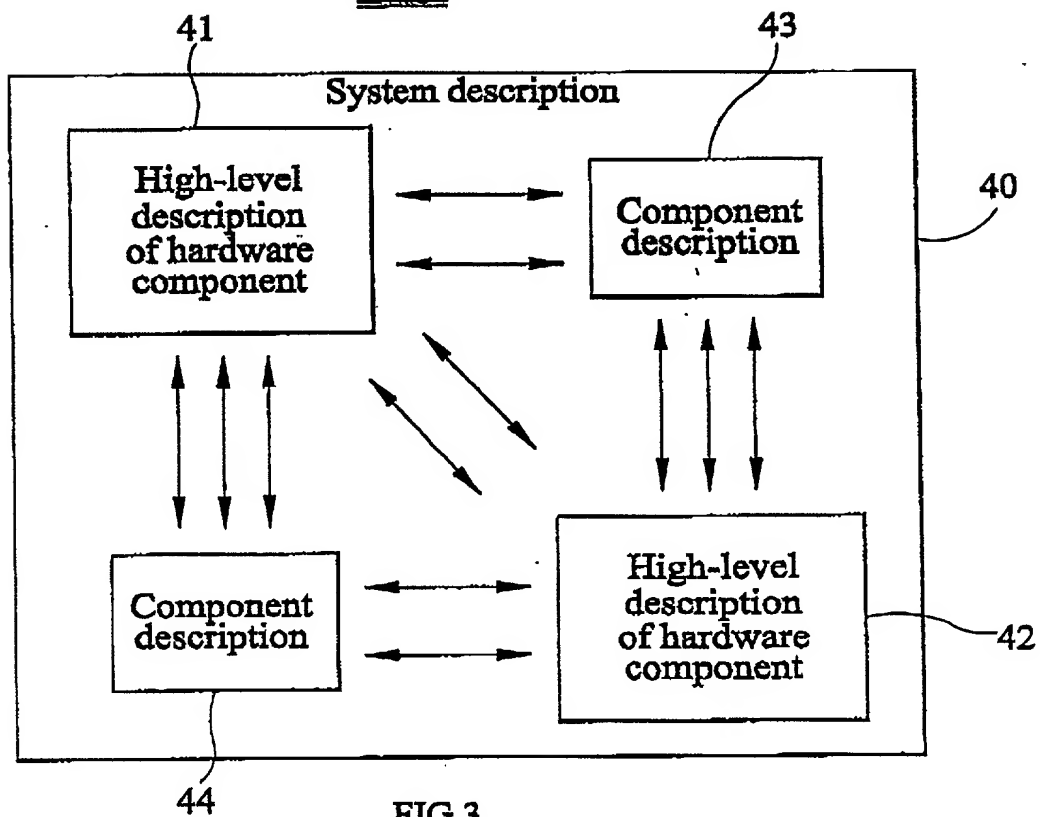
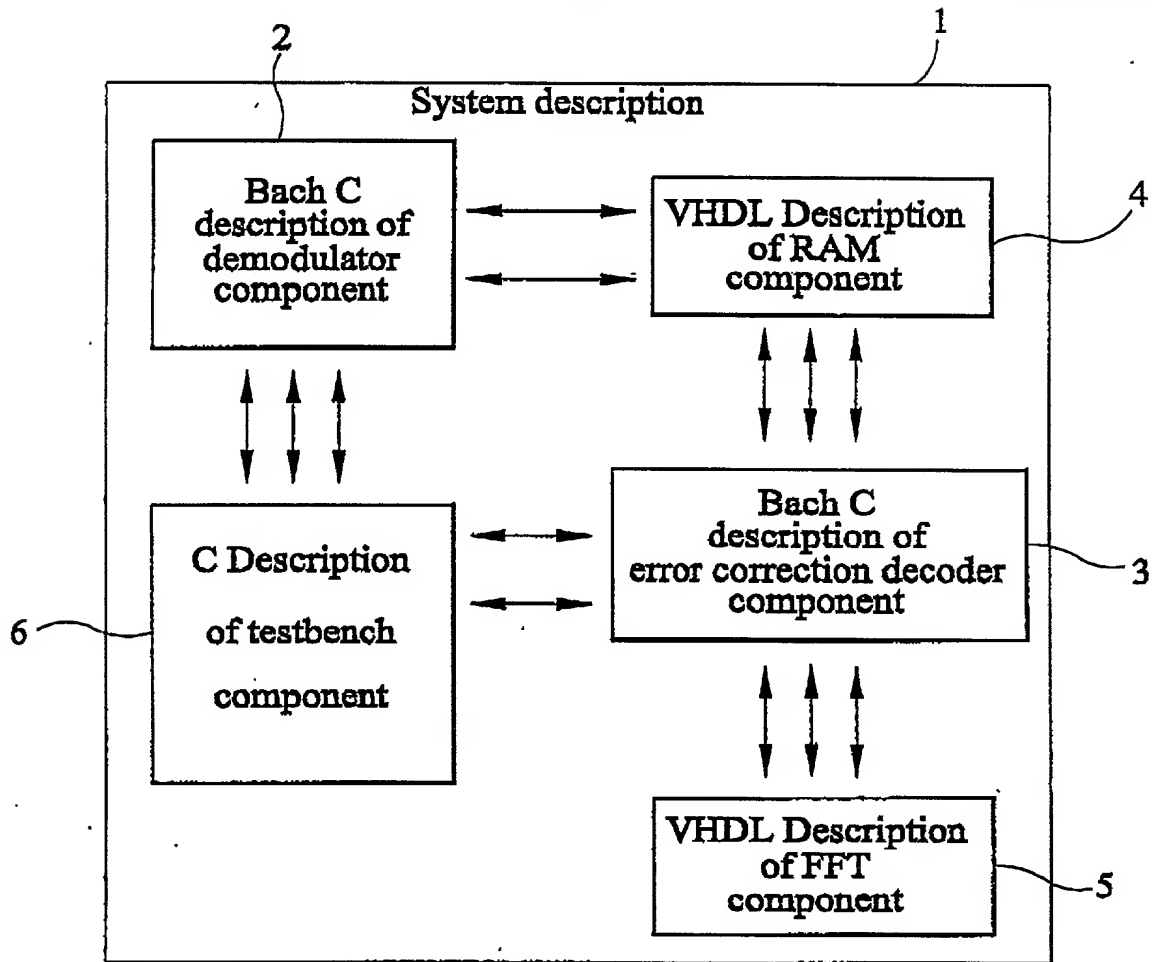
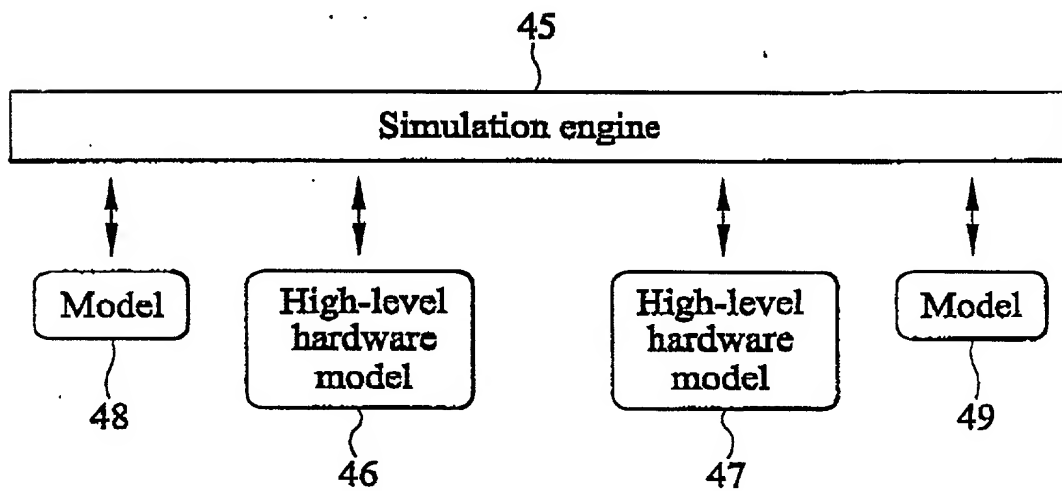


FIG.3

FIG. 4FIG. 5

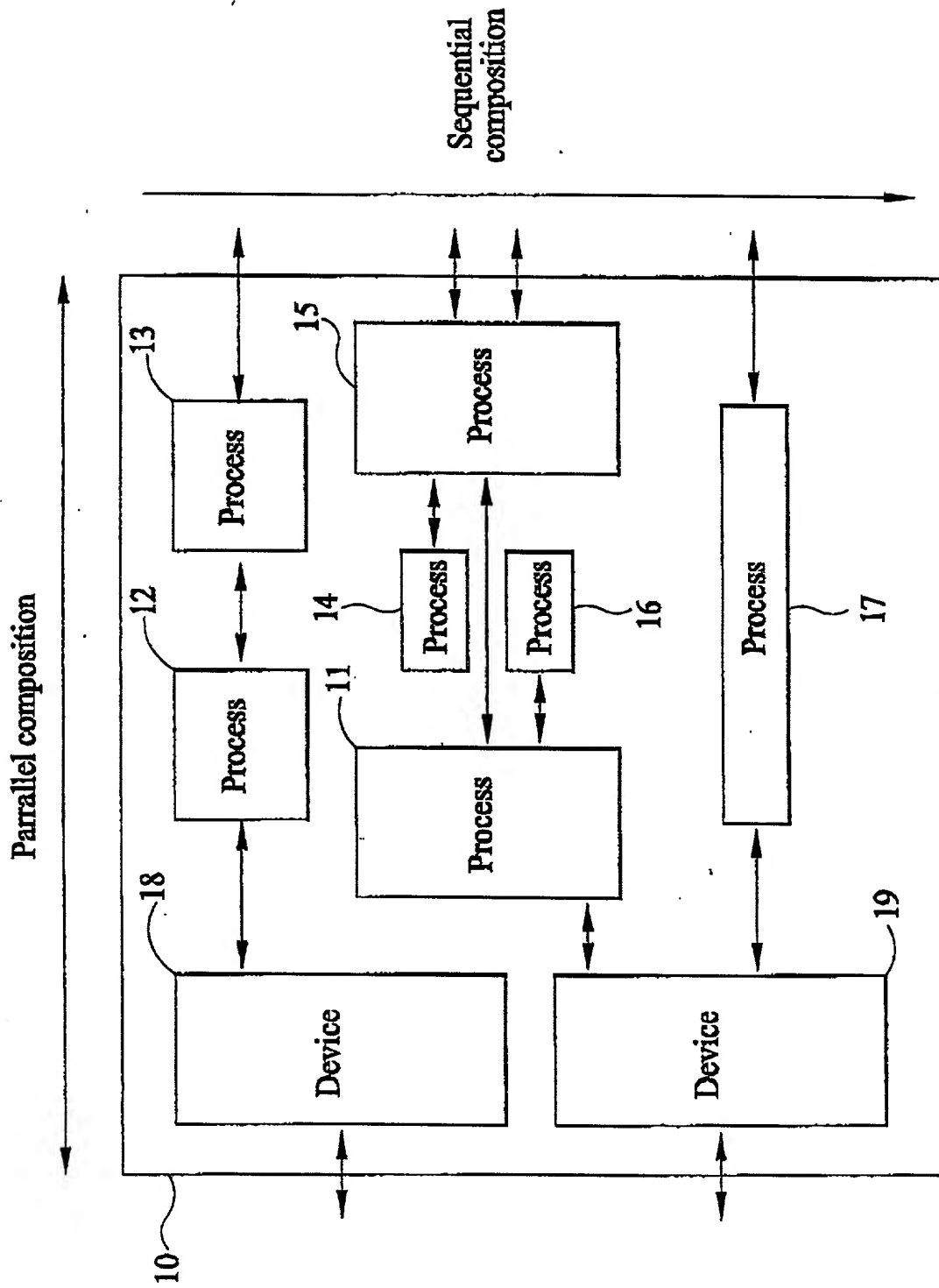
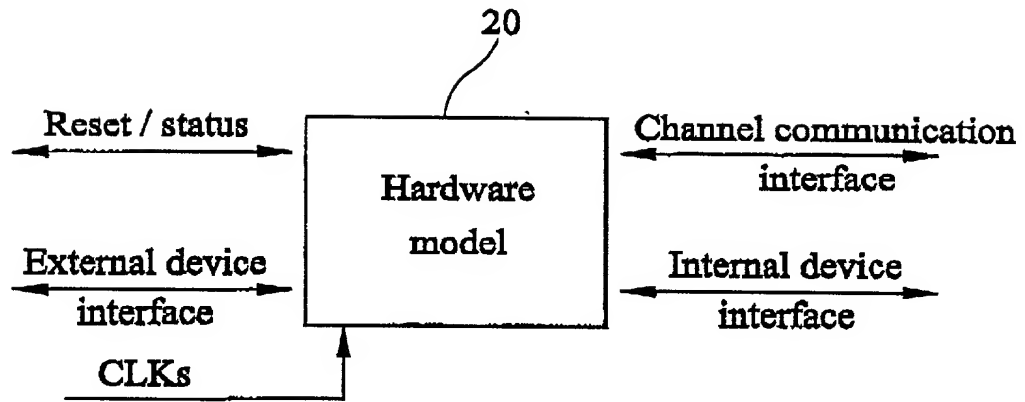
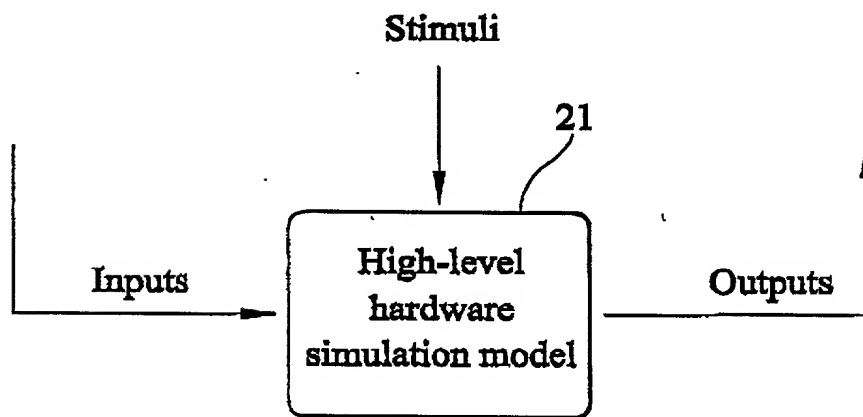
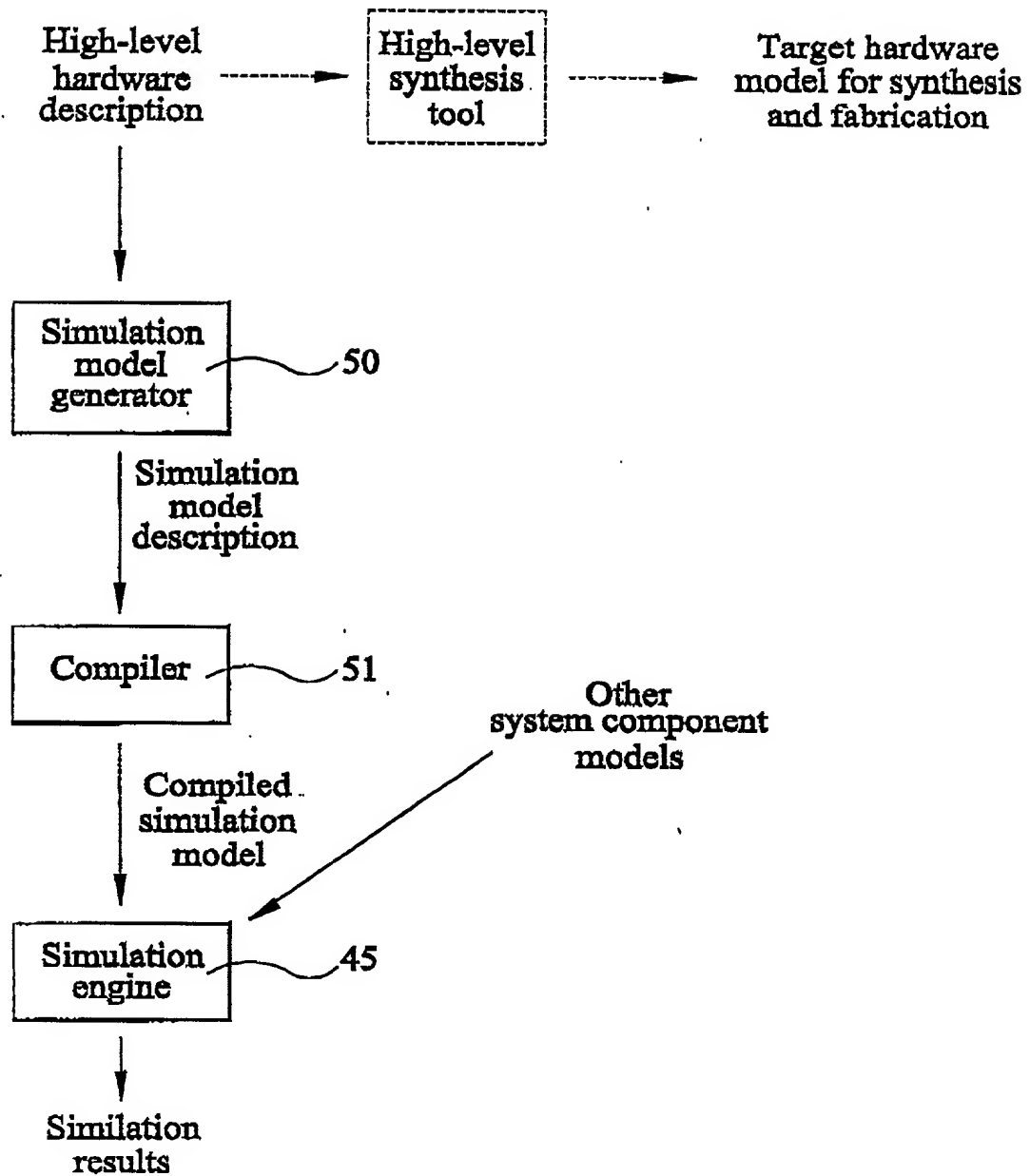
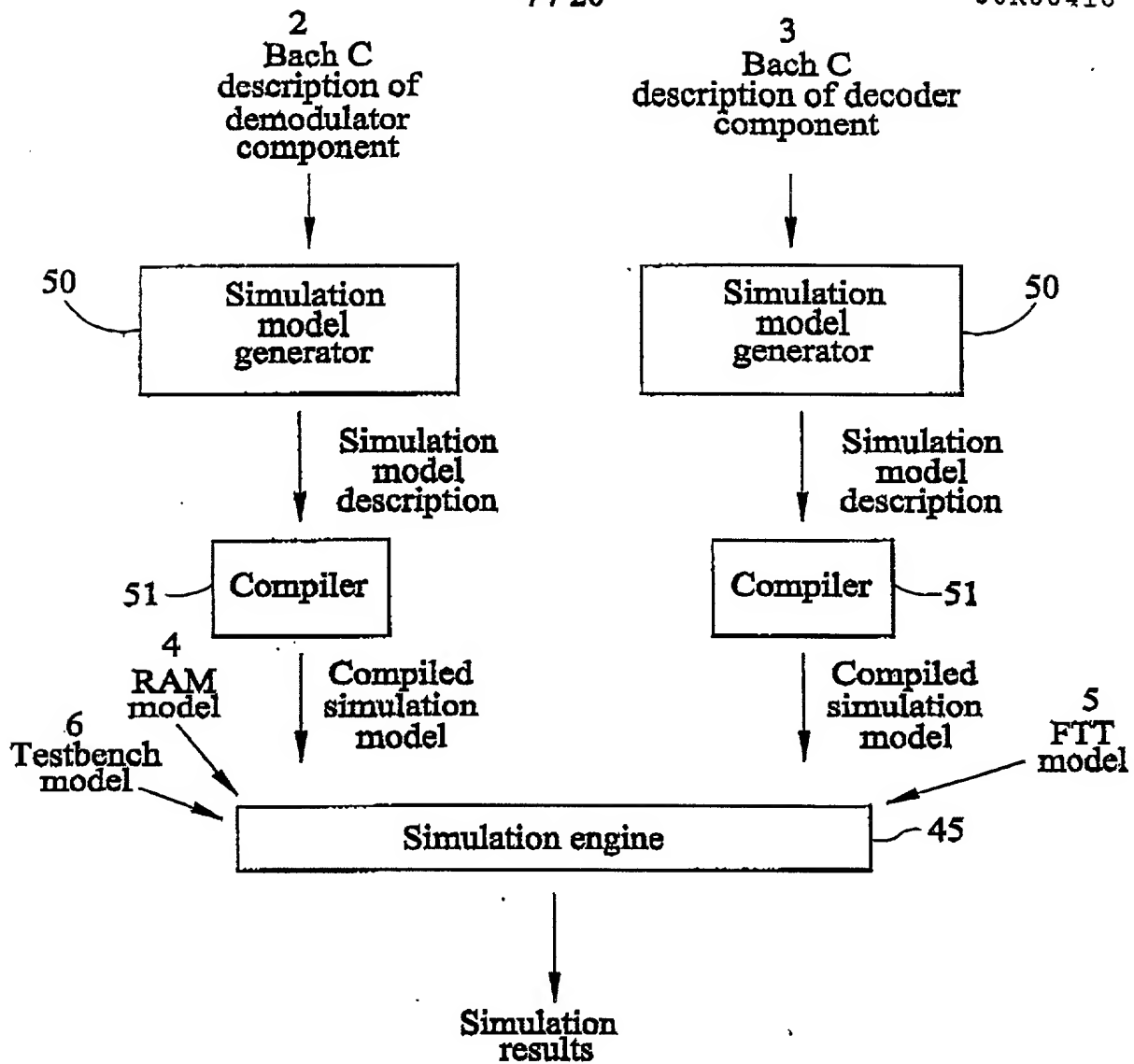
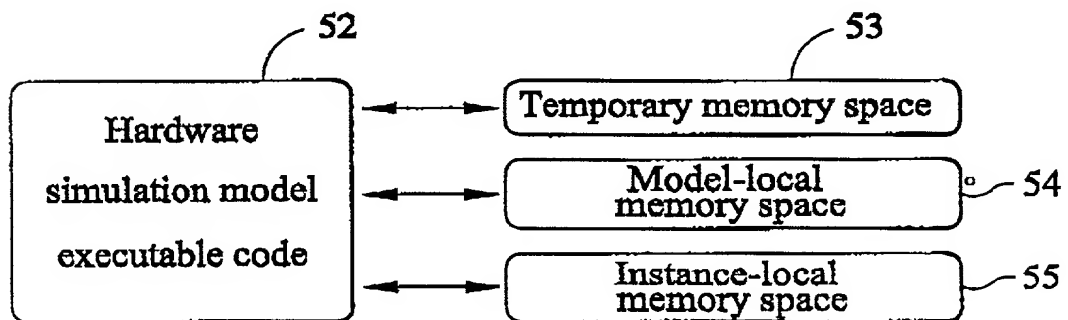
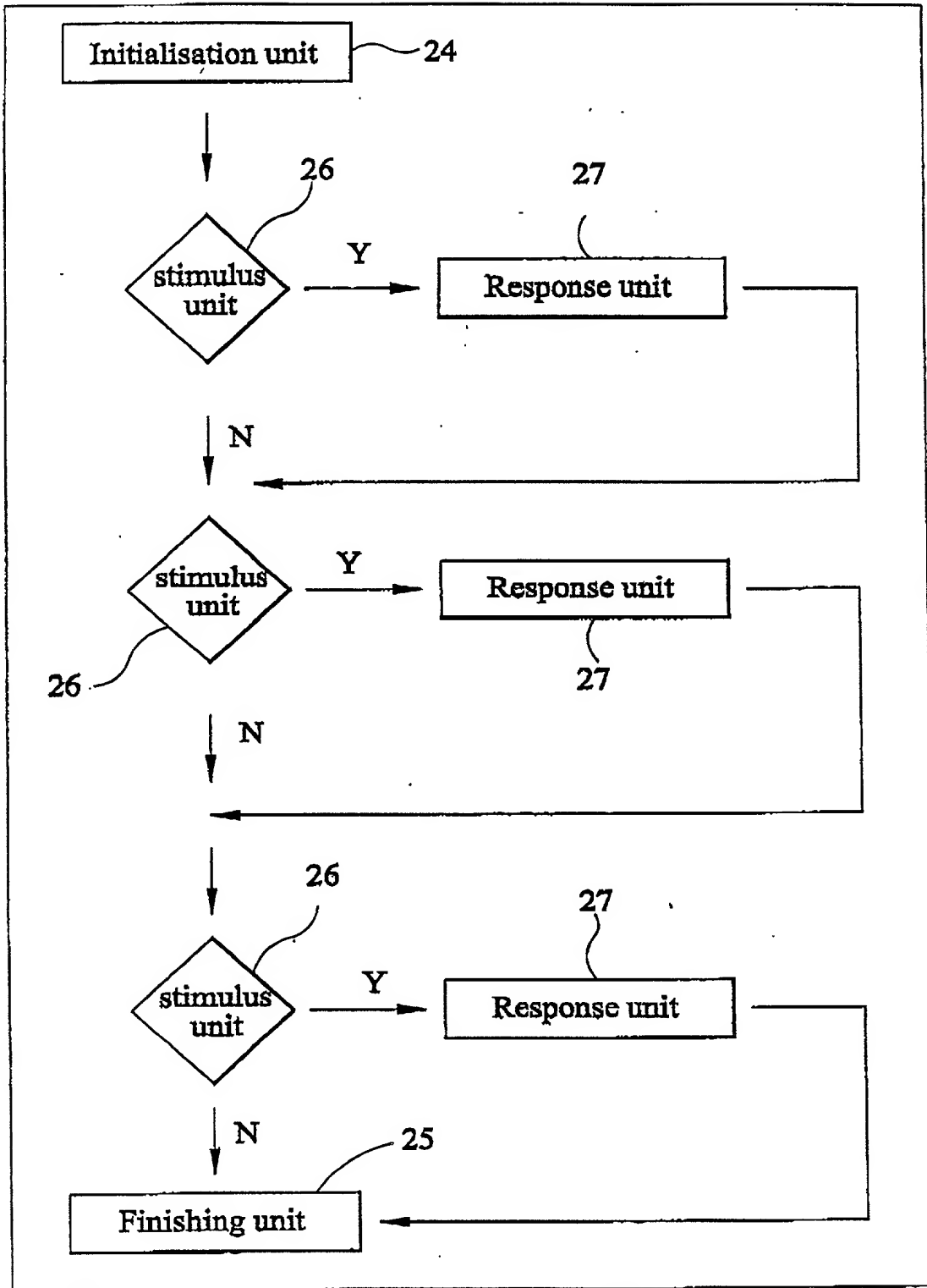


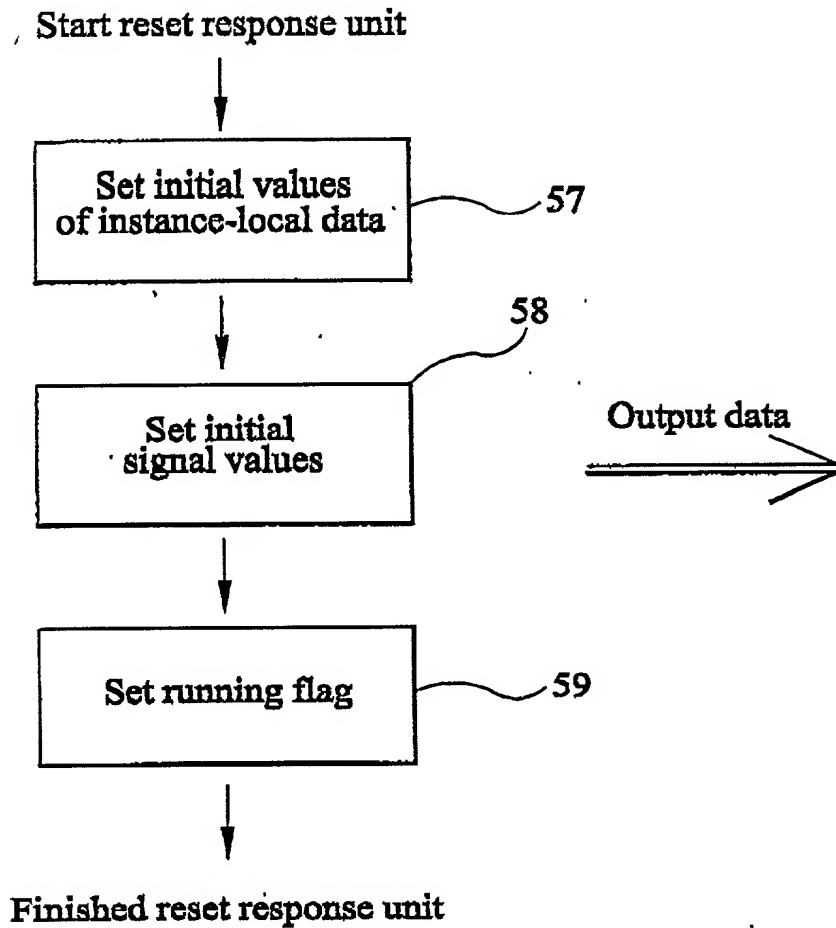
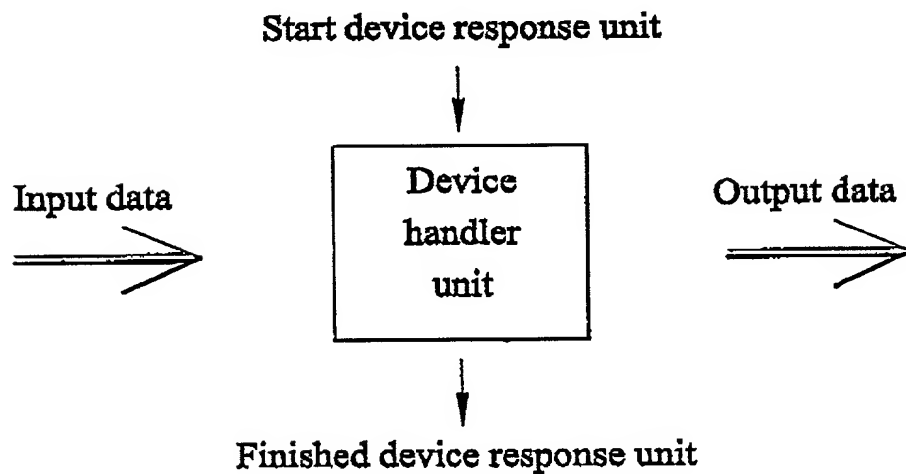
FIG.6

FIG.7FIG.8

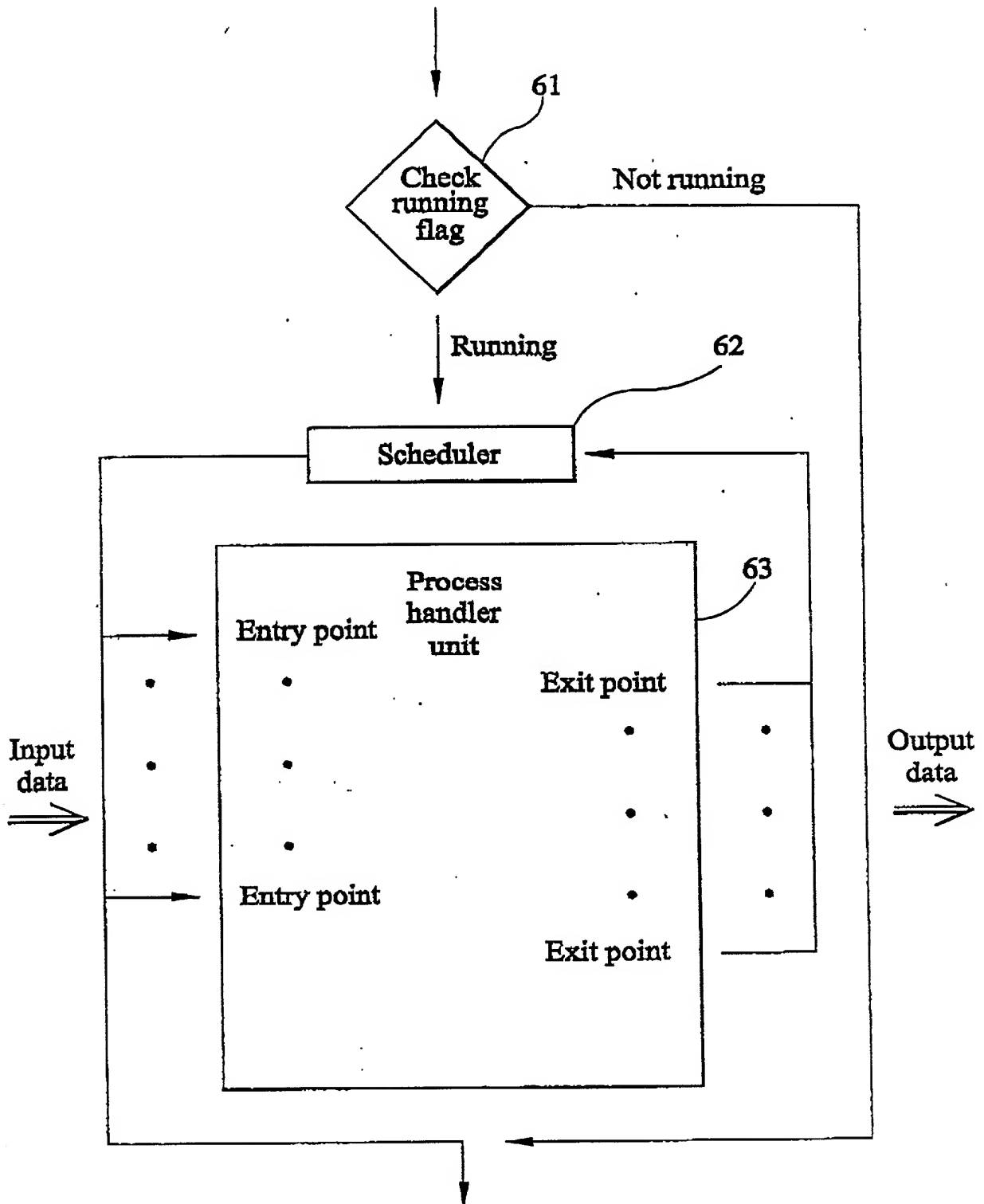
FIG.9

FIG.10FIG.11

FIG.12

FIG.13FIG.14

Start process response unit



Finished process response unit

FIG.15

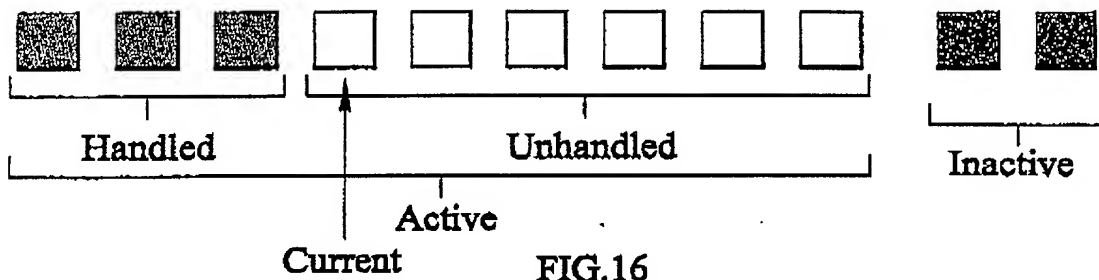


FIG.16

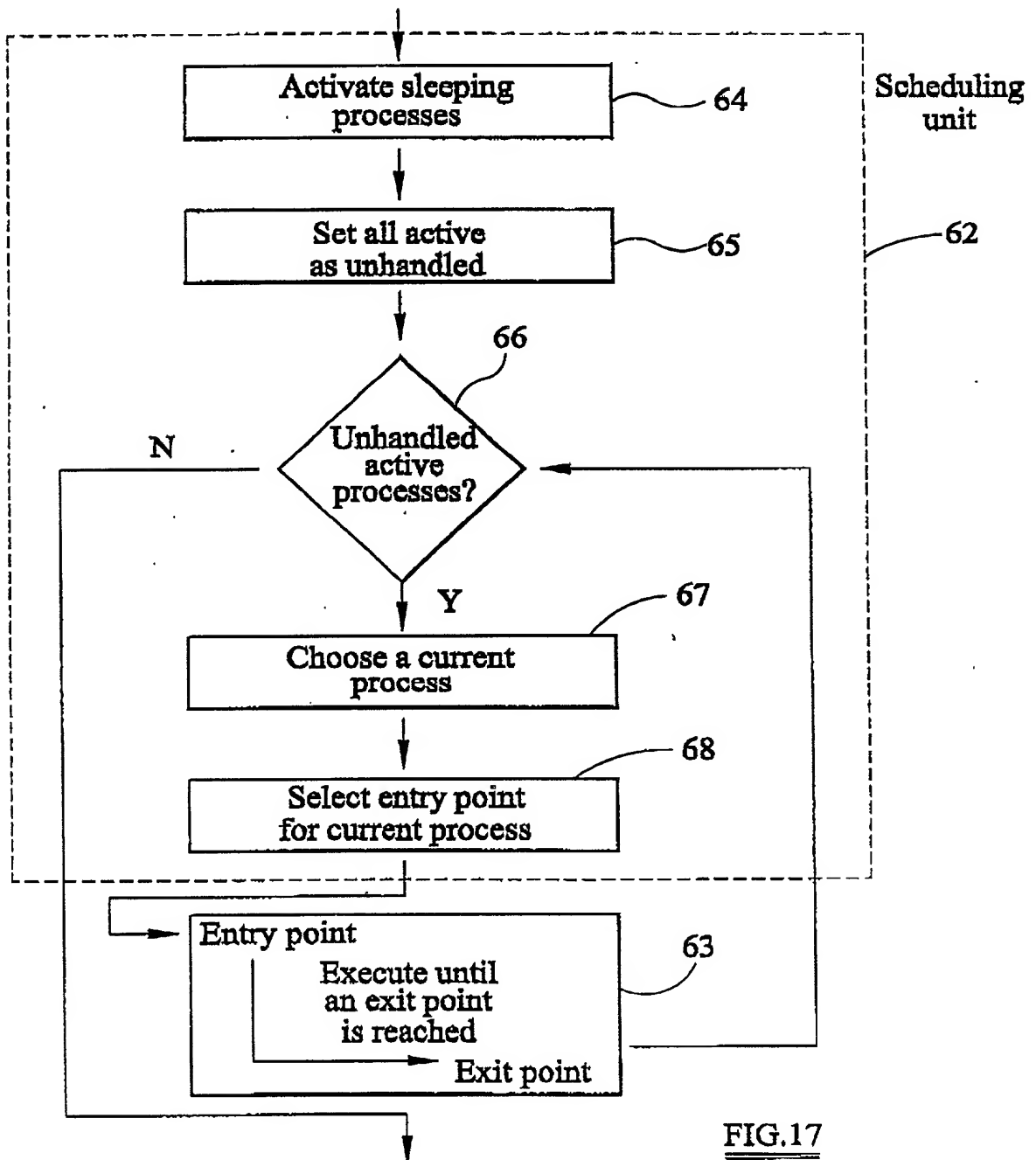
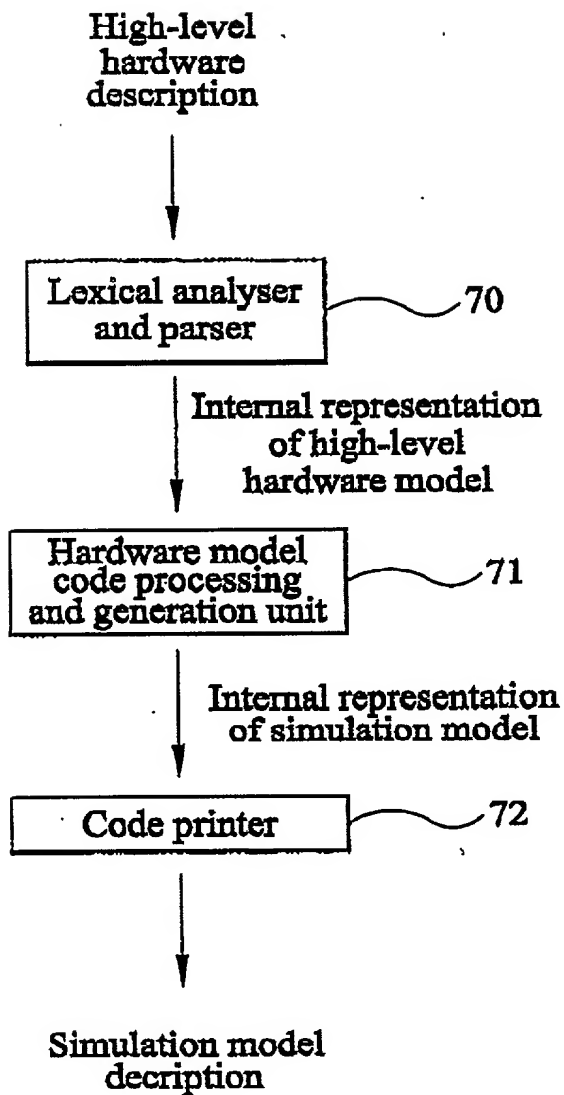
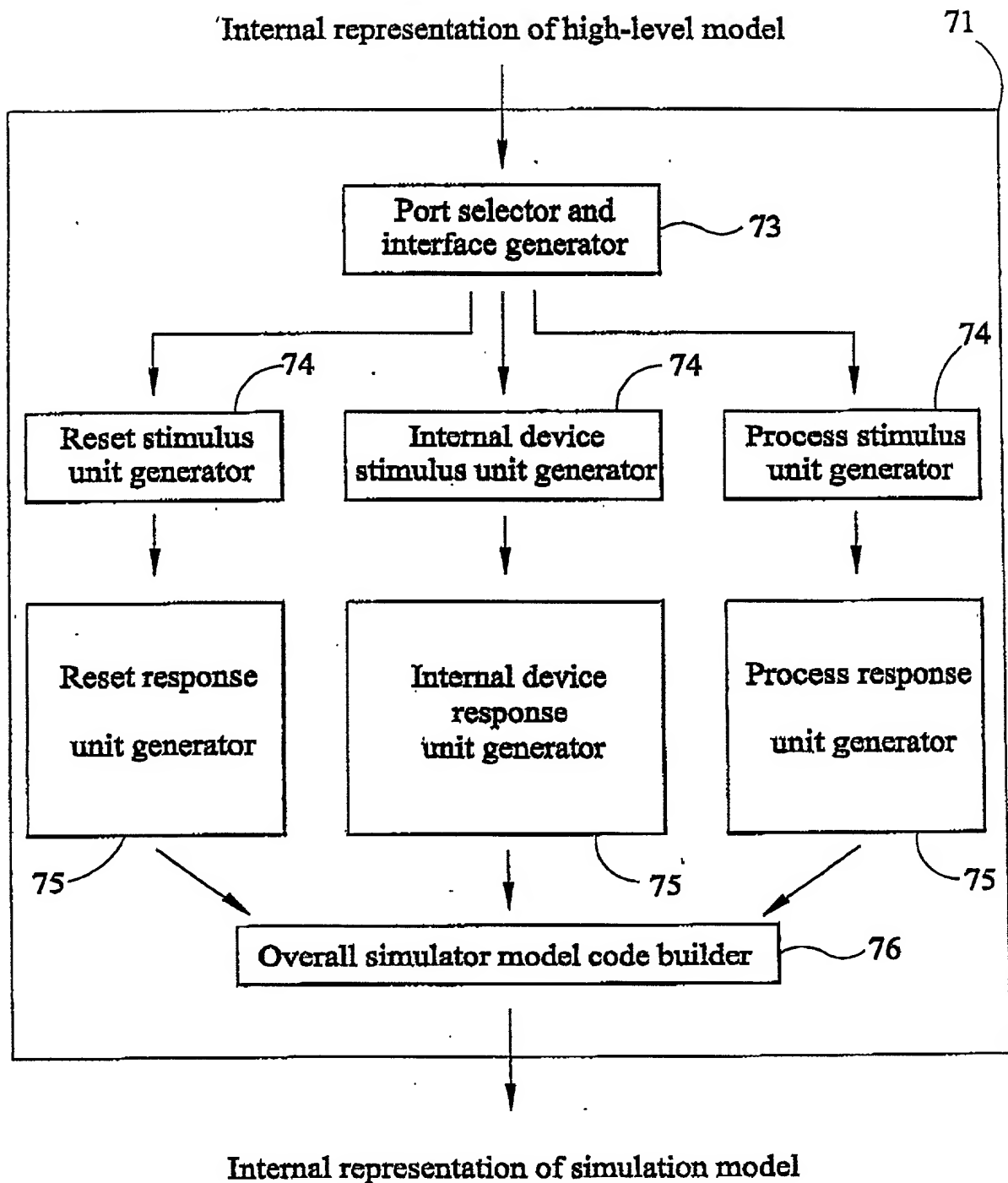
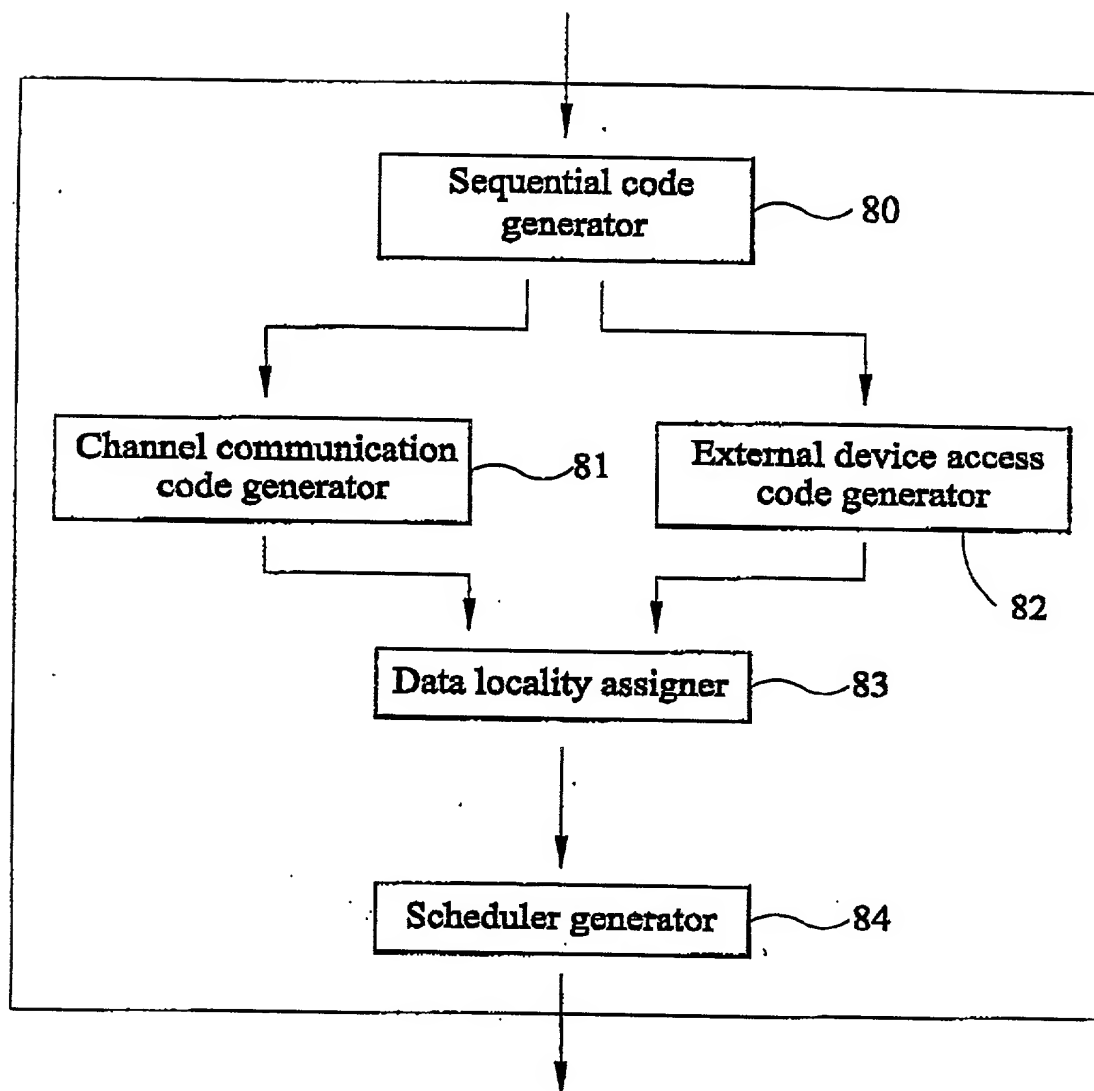
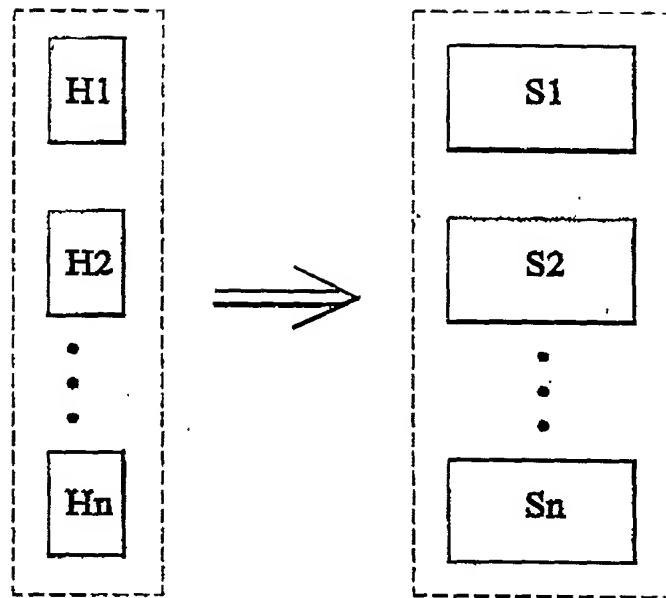
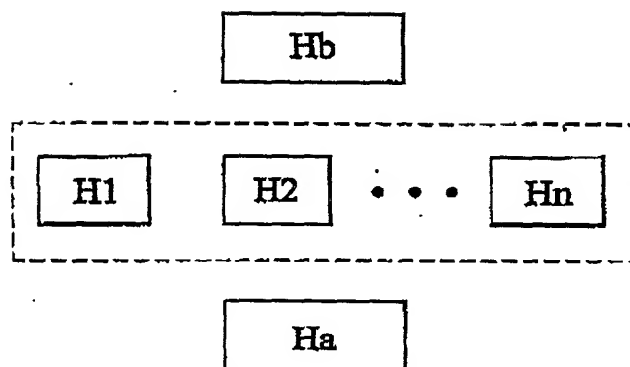


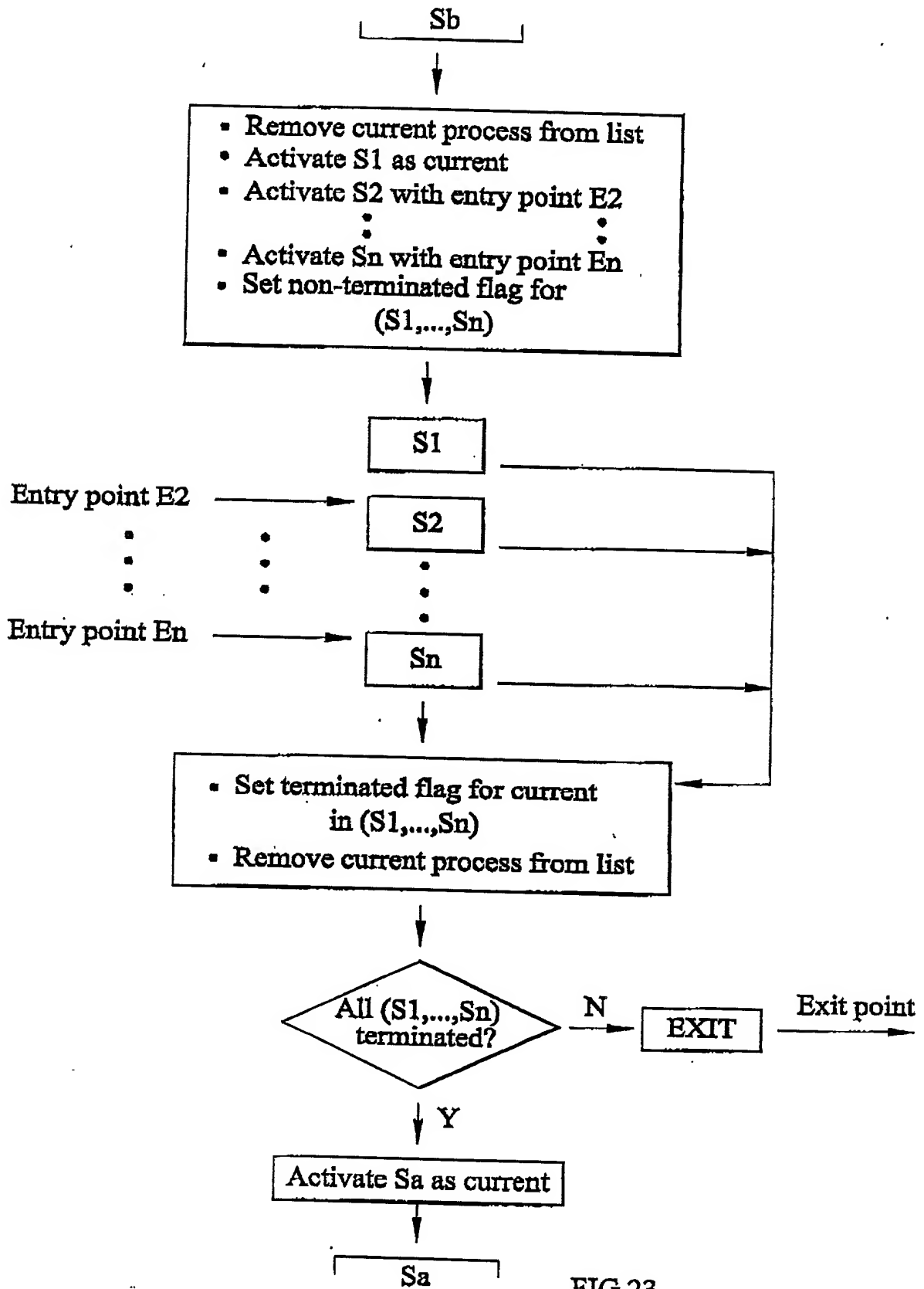
FIG.17

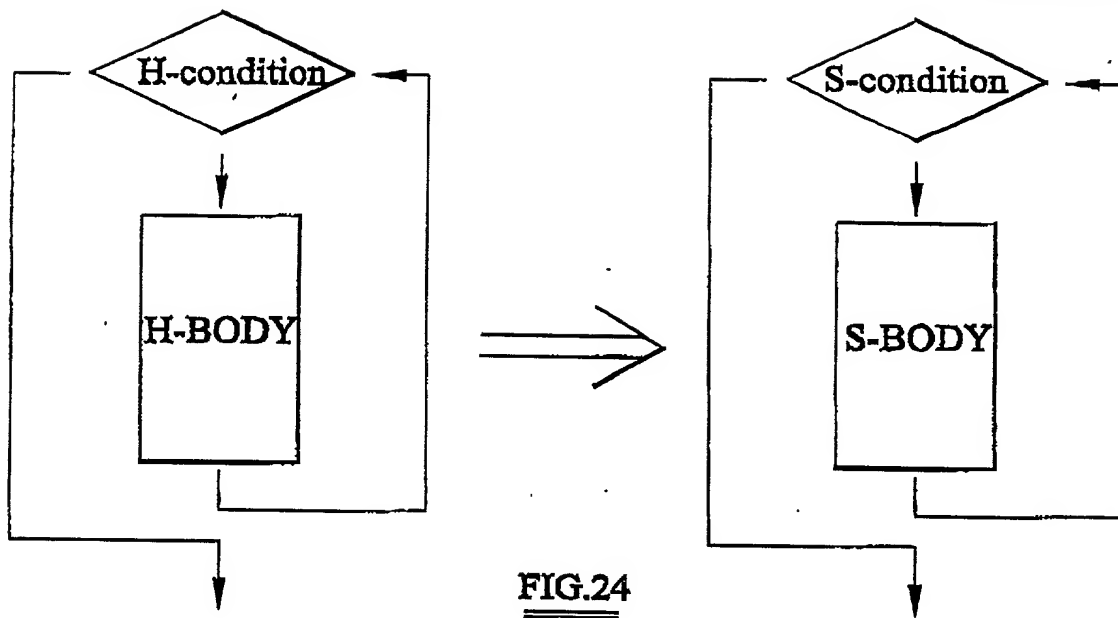
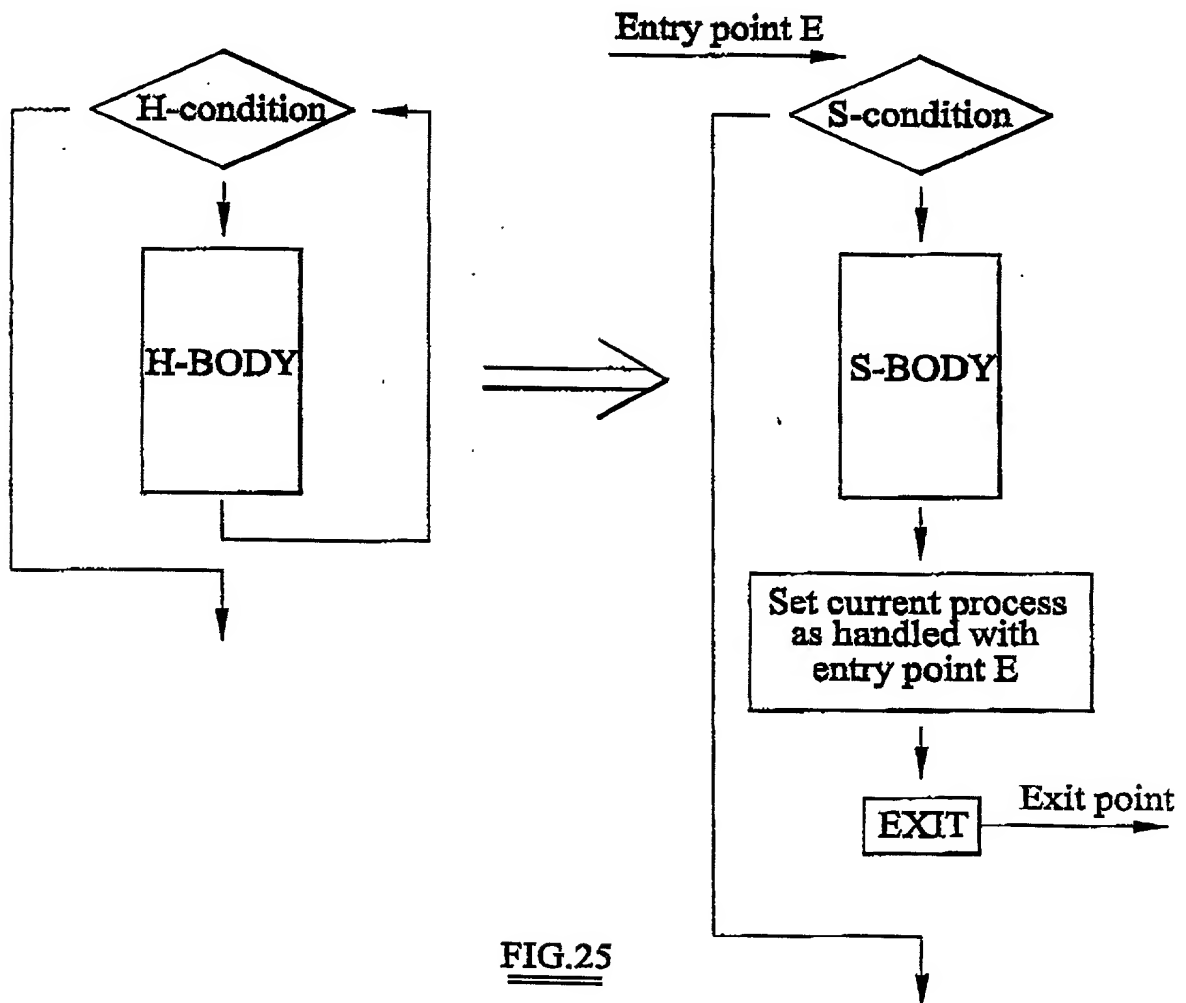
FIG.18

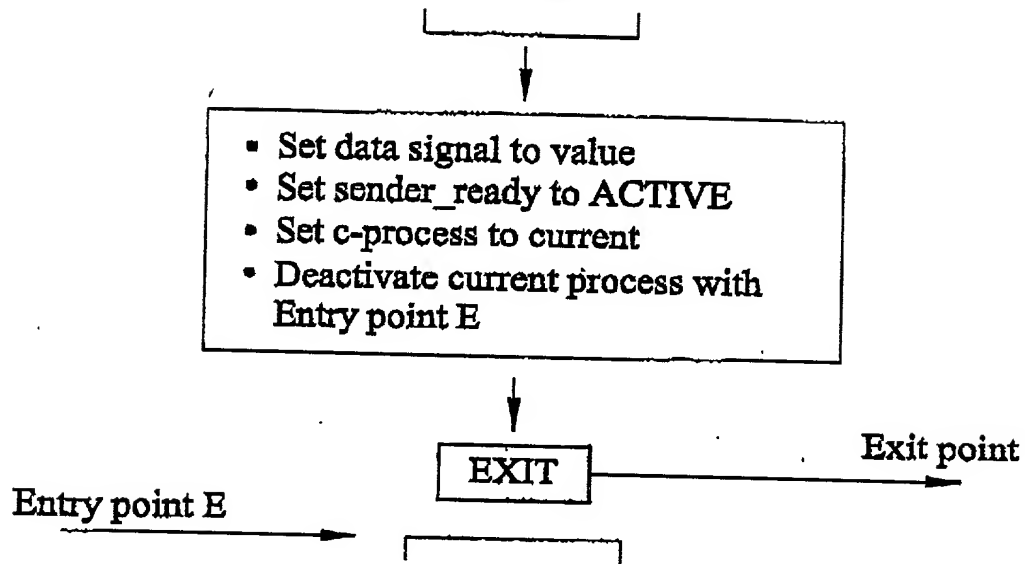
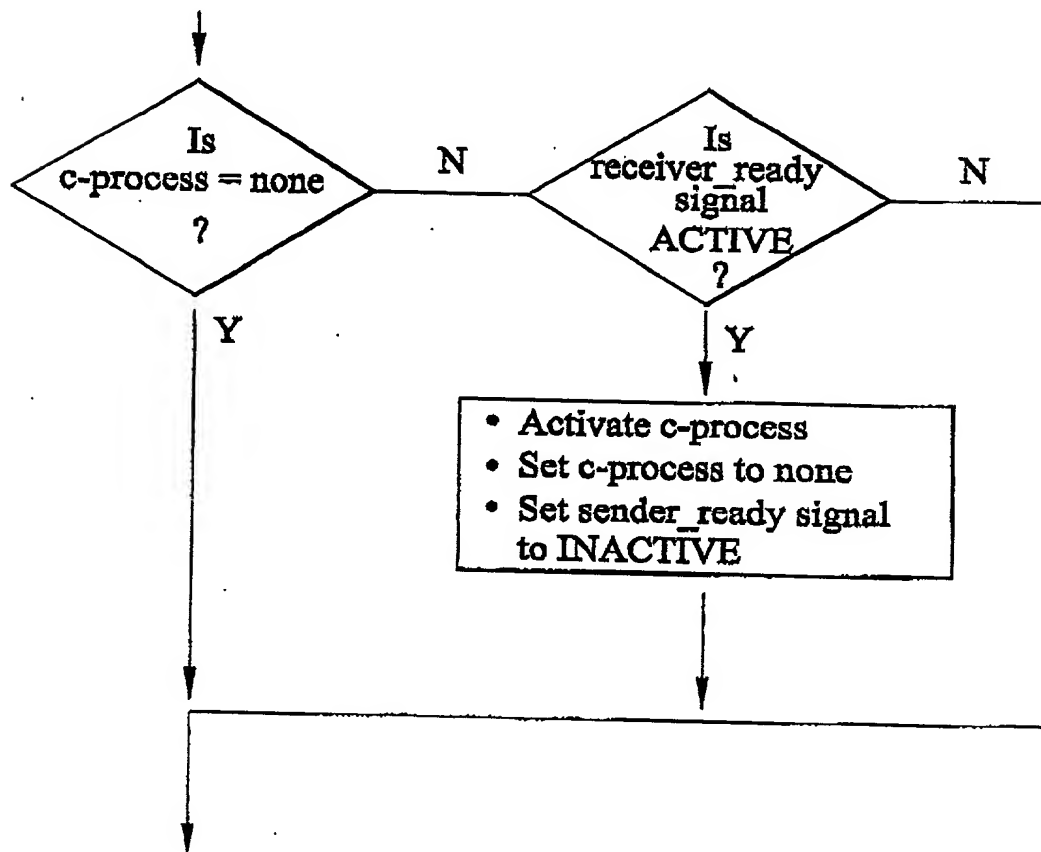
FIG.19

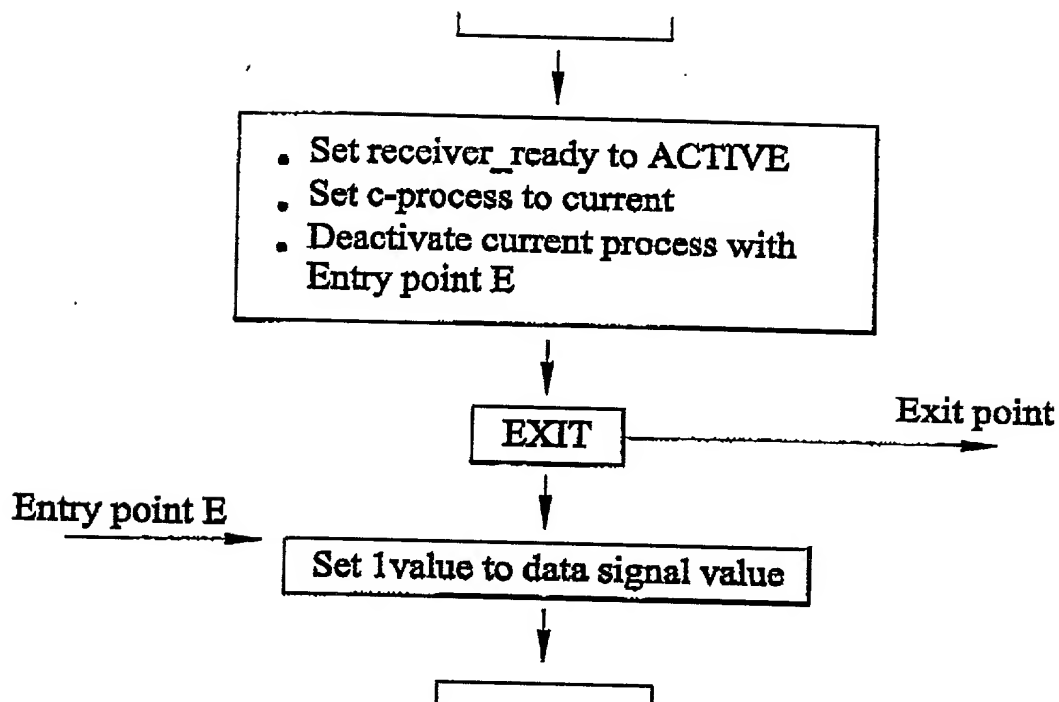
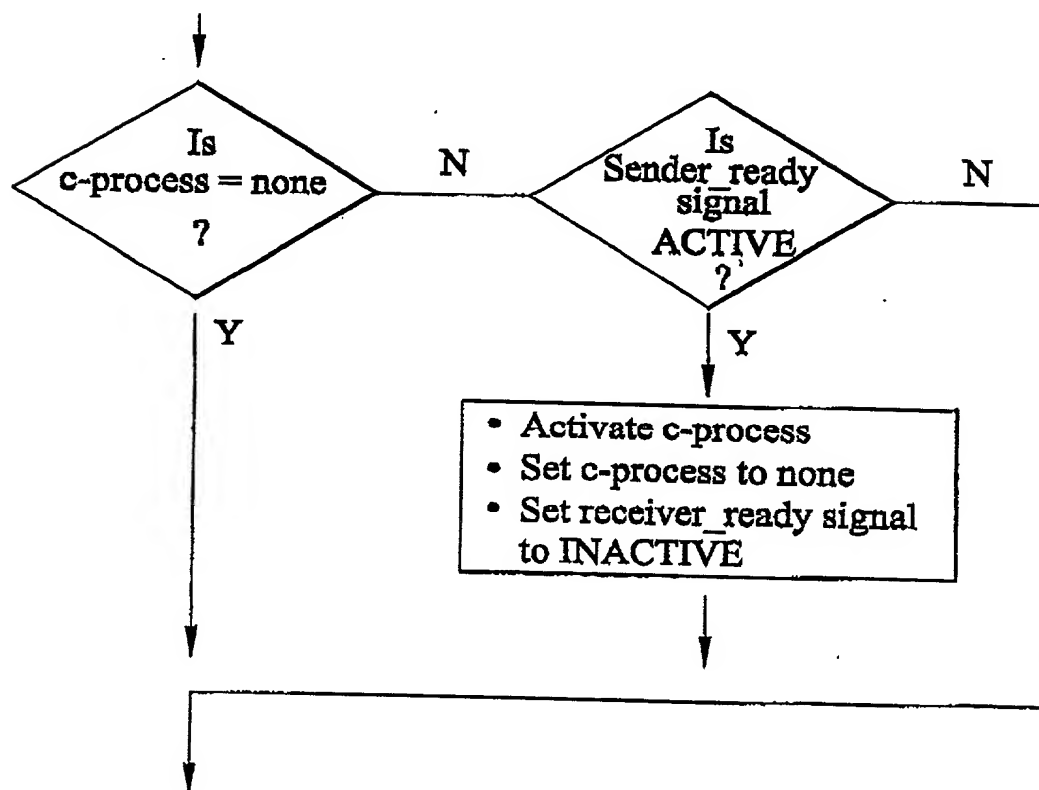
FIG.20

FIG.21FIG.22

FIG.23

FIG. 24FIG. 25

FIG.26FIG.27

FIG.28FIG.29



No need for instance local data

Need for instance local data

FIG.30